

Remarks

Reconsideration and further examination is respectfully requested. Claims 1-25 were originally presented for examination. Claims 1, 3-10, 12-17 and 19-25 were amended in a reply to a First Office Action. New claims 26 and 27 were added in a reply to a Second Office Action. Claims 10-16 and 26-27 have been cancelled without prejudice. Claims 1-9 and 17-25 are presented for further examination. The Examiner has indicated Allowability of claims 1-9 and 17-25.

The Examiner has stated that the Title of the invention is not sufficiently descriptive. The Title was amended in reply to the Second Office Action. The amended title is again presented and Examiner's consideration of the amended title is respectfully requested.

The Examiner has asserted that Figure 1 in the drawings should be labeled as prior art. The Examiner has cited Figure 1B of Lin (US 5,581,562) as teaching or suggesting the methods depicted in Figure 1 of the present invention.

Lin shows a design flow where an architectural definition provides an input to a behavioral simulation. This requires that the architectural definition be a behavioral description and employ a behavioral language. Logic is then generated from the behavioral simulation. It is noted that Lin does not provide a description of the numbered elements of the cited figure.

Figure 1 of the present invention sets forth a design process. A behavioral description, as required by Lin, is not an element of Figure 1 of the present invention, or of the claims. Further, Lin does not show "partitioning a design into a plurality of functional blocks" or "converting said first block design from Verilog to SPICE" as shown in Figure 1 (and recited in claims 1 and 17). Hence, Figure 1 is not prior art.

Conclusion

Since only the allowed claims 1-9 and 17-25 are now presented, and the other claims 10-16 and 26-27 have been cancelled without prejudice, this application is considered to be in condition for allowance and such action as earnestly solicited.

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Respectfully submitted,



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